IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (PREVIOUSLY PRESENTED) A microcontroller, comprising:

a mode terminal receiving a mode signal to distinguish a normal operation mode and a rewrite operation mode;

an internal nonvolatile memory storing therein a program to be executed during said rewrite operation mode;

a CPU core generating address signals sequentially, activating a first chip select signal when the address signals designate a first area, activating a second chip select signal when the address signals designate a second area, receiving, during said rewrite operation mode, rewrite data according to the program stored in said internal nonvolatile memory, and writing the received rewrite data to an electrically rewritable internal volatile memory connected to the microcontroller;

a selector circuit receiving the mode signal at a select terminal thereof, transmitting the first chip select signal to an external nonvolatile memory and transmitting the second chip select signal to an external volatile memory connected to the microcontroller when the mode signal indicates said normal operation mode, and

receiving the mode signal at a select terminal thereof, transmitting a first chip select signal to an internal nonvolatile memory and transmitting the second chip select signal to said external nonvolatile memory when the mode signal indicates said rewrite operation mode.

2. (PREVIOUSLY PRESENTED) The microcontroller according to claim 1, wherein:

said internal volatile memory stores in advance therein a transfer program for transferring to said internal volatile memory the rewrite data to be written to said external nonvolatile memory and a rewrite program for writing the rewrite data to said external nonvolatile memory; and

during said rewrite operation mode, said CPU core transfers the rewrite data to said internal volatile memory by executing said transfer program, and writes the transferred rewrite data to said external nonvolatile memory by executing said rewrite program.

3. (PREVIOUSLY PRESENTED) The microcontroller according to claim 1,wherein:

said internal volatile memory stores in advance therein a transfer program for transferring, to said internal volatile memory, the rewrite data to be written to said external nonvolatile memory and a rewrite program for writing the rewrite data to said external nonvolatile memory; and

said CPU core transfers the rewrite data and said rewrite program to said internal volatile memory by executing said transfer program, and writes the rewrite data, transferred to said internal volatile memory, to said external nonvolatile memory by executing the rewrite program transferred to said internal volatile memory.

4. (PREVIOUSLY PRESENTED) The microcontroller according to claim 1, further comprising:

a selector control circuit forcibly outputting, to said selector circuit, a level indicating said normal operation mode,based on a control signal from the CPU core.

5. (CANCELLED)

6. (CANCELLED)

7. (PREVIOUSLY PRESENTED) The microcontroller according to claim 1, further comprising:

an interface circuit receiving the rewrite data to be written to said external nonvolatile memory via an external terminal; andsaid CPU core controlling said interface circuit according to said program to receive the rewrite data.

8. (PREVIOUSLY PRESENTED) The microcontroller according to claim 7, further comprising:

an internal volatile memory accessed by said CPU core; and said CPU core transferring the rewrite data to said internal volatile memory via said interface circuit during said rewrite operation mode.

9. (PREVIOUSLY PRESENTED) The microcontroller according to claim 1, wherein:

said CPU core generates an address signal which designates a first area initially after power-on.